



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,500	10/16/2000	Kenneth J. Kledzik	LE99-02	3227
75	10/02/2002			
RANDALL L. REED			EXAMINER	
LEVIN AND HAWES, LLP 384 FOREST AVE.			ALCALA, JOSE H	
SUITE 13			ART UNIT	PAPER NUMBER
LAGUNA BEA	ACH, CA 92652		2827	
		DATE MAILED: 10/02/2002		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	7			
.,,	09/688,500	KLEDZIK ET AL.				
Office Action Summary	Examiner	Art Unit	7			
	Jose H Alcala	2841				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM						
THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed						
Extensions of time may be available under the provided in a provided in a first SIX (6) MONTHS from the mailing date of this communication.  If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).  Status						
1) Responsive to communication(s) filed on 1	<u> 1 December 2001</u> .					
2a)☐ This action is FINAL. 2b)⊠	2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) 1-34 is/are pending in the application.						
4a) Of the above claim(s) 7-12,19-23, and 30-34 is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-6,13-18 and 24-29</u> is/are rejected.						
7) Claim(s) is/are objected to.	5					
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)⊠ The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on 16 October 2000 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Applicant may not request that any objection t	o the drawing(s) be need	d h\□ disapproved by the Examiner.				
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) All b) Some * c) None of:						
<ul> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> </ul>						
2. Certified copies of the priority documents have been received in Approximation ———  3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (FC) Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) The translation of the foreign language provisional application has been received.  15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-94 3) Information Disclosure Statement(s) (PTO-1449) Paper N	4)	Interview Summary (PTO-413) Paper No(s)  Notice of Informal Patent Application (PTO-152)  Other:				

Art Unit: 2841

#### **DETAILED ACTION**

Page 2

#### Election/Restrictions

- 1. Applicant's election without traverse of Species 1 in Paper No. 5 is acknowledged.
- 2. Claim 7-12,18-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non elected Species, there being no allowable generic or linking claim. Election was made without traverse in Paper No. 5.

### **Drawings**

- 3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference number 301 is not in Figure 1. Reference numbers 105H, 105E and 104H are not in Figure 3. Reference number 402 is not in Figure 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- 4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference number 106 and 305 in Figure 5. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Art Unit: 2841

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "integrated circuit chip embedded within" a package body of each IC package must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### Specification

6. The disclosure is objected to because of the following informalities: Reference number 304 is used in Page line 17 to label "contact pads" and later is used in page 10, line 7 to label "heat sink layers". It is unclear if those are just two ways of calling the same elements or if the same reference number is designating two elements. In addition, in page 9, line 15 the word: "completely" is misspelled.

Appropriate correction is required.

### Claim Objections

7. Claims 1 is objected to because of the following informalities: In line 6, replace "mounting arrays" by --mounting pad arrays --, in order to avoid any confusion and have consistency in the language of the claim. Appropriate correction is required.

# Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Page 4

Application/Control Number: 09/688,500

Art Unit: 2841

9. Claims 1-6,13-17 and 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, line 6 reads: "coupled to a carrier interface". It is not clear if the recitation "carrier interface" is just another name for the carrier or for the mounting pad arrays, or if it is a separate element. If it is a separate element, there might be a 35 U.S.C. 112 first paragraph issue.

Claim 2 recites the limitation "the leads" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is suggested to change it to: --connection elements-- to be consistent with Claim 1.

Regarding Claim 13, line 8 reads: "interface coupled". It is not clear if the recitation "interface coupled" is just another name for the mounting pad array, or if it is a separate element. If it is a separate element, there might be a 35 U.S.C. 112 first paragraph issue.

Regarding Claim 24, line 8 reads: "carrier interface". It is not clear if the recitation "carrier interface" is just another name for the carrier, or if it is a separate element. If it is a separate element, there might be a 35 U.S.C. 112 first paragraph issue.

# Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

<sup>(</sup>b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2841

11. Claims 1-3,5 are rejected under 35 U.S.C. 102(b) as being anticipated by Coller et al. (US Patent No. 4,696,525). As best understood by the examiner:

Regarding Claim 1, Coller teaches an electronic circuit module comprising: at least one IC package unit, each unit having a carrier (Reference Number 30) having first and second IC package mounting locations (Reference Numbers 50 and 52, respectively) on opposed sided thereof, said first mounting location (Reference Number 50) having a first mounting pad array (Reference Number 78), said second mounting location (Reference Number 52) having a second mounting pad array (Reference Number 86), said first and second mounting arrays being coupled to a carrier interface; and a pair of IC packages (Reference Numbers 100A and 100B), each package having a package body (Reference Number 104) containing an integrated circuit chip and a plurality of connection elements (Reference Number 112) coupled to said chip and extending at least to the surface of said body, the connection elements of said first package being conductively bonded to said first mounting pad array (See Figure 3), the connection elements of said second package being conductively bonded to said second mounting pad array (See Figure 3); and a printed circuit board (Reference Number 130) having at least one interconnection pad array (Reference Number 134) affixed thereto, each interconnection pad array coupled to circuitry (Reference Number 132) on the printed circuit board and conductively bonded to the interface of a single IC package unit (See Figure 3).

Regarding Claim 2, Coller teaches that individual mounting pads of said first mounting pad array (Reference Number 78) are coupled to individual mounting pads of

Art Unit: 2841

said second mounting pad array (Reference Number 86) by means of conductive links (Reference Number 70) within the carrier (Reference Number 30), and the leads (Reference Number 112) of one of said IC packages are conductively bonded directly to said interconnection pad array (See bottom of Figure 3).

Regarding Claims 3 and 5, Coller teaches that the carrier (Reference Number 30) comprises a plastic body (Reference number 54) having first and second major planar faces corresponding, respectively, to said first and second IC package mounting locations (See Figure 1), where the IC packages fit tightly between end walls (Reference Numbers 35 and 36). Thus, it is inherent that the plastic body is a flexible polymeric film or a semi-rigid laminar substrate.

12. Claims 13-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Coller et al. (US Patent No. 4,696,525). As best understood by the examiner:

Regarding Claim 13, Coller teaches an electronic circuit module comprising: at least one pair of IC packages (Reference Numbers 100A and 100B), each package having a package body (Reference Number 104), an integrated circuit chip embedded within said body, and a plurality of connection elements (Reference Number 112) coupled to said chip which extend at least to the surface of said body; one package carrier (Reference Number 30) for each IC package pair, each carrier having two opposing major faces (top and bottom surfaces of Reference Number 30), each face having a mounting pad array (top face has Reference Number 78, bottom face has Reference Number 86) to which the connection elements of one IC package of each package pair are conductively bonded (For example see Reference Number 80), each

Art Unit: 2841

carrier having an interface (Reference number 62) coupled to the connection elements of both IC packages; and a printed circuit board (Reference Number 130) having at least one interconnection pad array (Reference Number 134) affixed thereto, each interconnection pad array conductively bonded to the carrier interface (See bottom of

Figure 3).

Regarding Claim 14, Coller teaches that the pairs of mounting pads on opposite major faces of said package carrier are electrically interconnected (See Reference number 70), and the connection elements (Reference Number 112) of one of said IC packages are conductively bonded directly to said interconnection pad array (See bottom of Figure 3).

Regarding Claims 15 and 17, Coller teaches that the carrier (Reference Number 30) comprises a plastic body (Reference number 54) having first and second major planar faces corresponding, respectively, to said first and second IC package mounting locations (See Figure 1), where the IC packages fit tightly between end walls (Reference Numbers 35 and 36). Thus, it is inherent that the plastic body is a flexible polymeric film or a semi-rigid laminar substrate.

13. Claims 24-26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Coller et al. (US Patent No. 4,696,525). As best understood by the examiner:

Regarding Claim 24, Coller teaches an electronic circuit module comprising: an IC package unit having a plurality of IC packages (Reference Numbers 100A and 100B), each package having a package body (Reference Number 104), an integrated circuit chip embedded within said body, and a plurality of connection elements

Art Unit: 2841

(Reference Number 112) coupled to said chip which extend at least to the surface of said body; a package carrier (Reference Number 30) having two opposing major faces (top and bottom surfaces of Reference Number 30), each face having at least one mounting pad array (top face has Reference Number 78, bottom face has Reference

Number 86) to which the connection elements of one IC package are conductively bonded (For example see Reference Number 80), each carrier providing a carrier interface (Reference number 62) coupled to the connection elements of the IC packages on that carrier; and a printed circuit board (Reference Number 130) having at least one interconnection pad array (Reference Number 134) affixed thereto, each interconnection pad array conductively bonded to the carrier interface (See bottom of Figure 3).

Regarding Claim 25, Coller teaches that the pairs of mounting pads on opposite major faces of said package carrier are electrically interconnected (See Reference number 70), and the connection elements (Reference Number 112) of one of said IC packages are conductively bonded directly to said interconnection pad array (See bottom of Figure 3).

Regarding Claims 26 and 28, Coller teaches that the carrier (Reference Number 30) comprises a plastic body (Reference number 54) having first and second major planar faces corresponding, respectively, to said first and second IC package mounting locations (See Figure 1), where the IC packages fit tightly between end walls (Reference Numbers 35 and 36). Thus, it is inherent that the plastic body is a flexible polymeric film or a semi-rigid laminar substrate.

Art Unit: 2841

## Claim Rejections - 35 USC § 103

- 14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 15. Claims 4,6,16,18,27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coller et al. (US Patent No. 4,696,525) in view of Levy et al. (US Patent No. 5,869,353). As best understood by the examiner:

Regarding Claims 4,6,16,18,27 and 29, Coller teaches all the limitations of the instant claimed invention as stated supra for Claims 3,5,13,17,24 and 28, but fails to teach that the circuit board includes a recess for each package unit affixed thereto, said recess receiving at least a portion of the body of one of said packages.

Levy teaches a circuit board (Reference Number 22) that includes a recess (Reference Number 24) for each package unit (Reference Number 12) affixed thereto, said recess receiving at least a portion of the body of one of said packages (See Figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Coller and Levy in order to include a recess to the circuit board, to receive at least a portion of the body of the IC packages. Thus, providing a way for the integrated circuit packages to be stacked, in order to achieve the desired electrical interconnections while being economical and easily reparable.

Art Unit: 2841

#### Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have some of the elements of the instant claimed invention, but fail to show the exact same arrangement of the elements:

Ishii (US Patent No. 5,744,862), Rosh (US Patent No. 6,222,737), Kledzik et al. (US Patent No. 6,313,998), Happoya et al. (US Patent No. 6,084,780), Derouiche (US Patent No. 5,754,408), Griffin et al. (US Patent No. 6,208,526) and Bechtel et al. (US Patent No. 5,182,632).

- 17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.
- 18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.
- 19. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA February 27, 2002

Klunes Drunay Examini